

REPLACEMENT SHEET

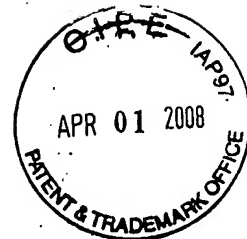
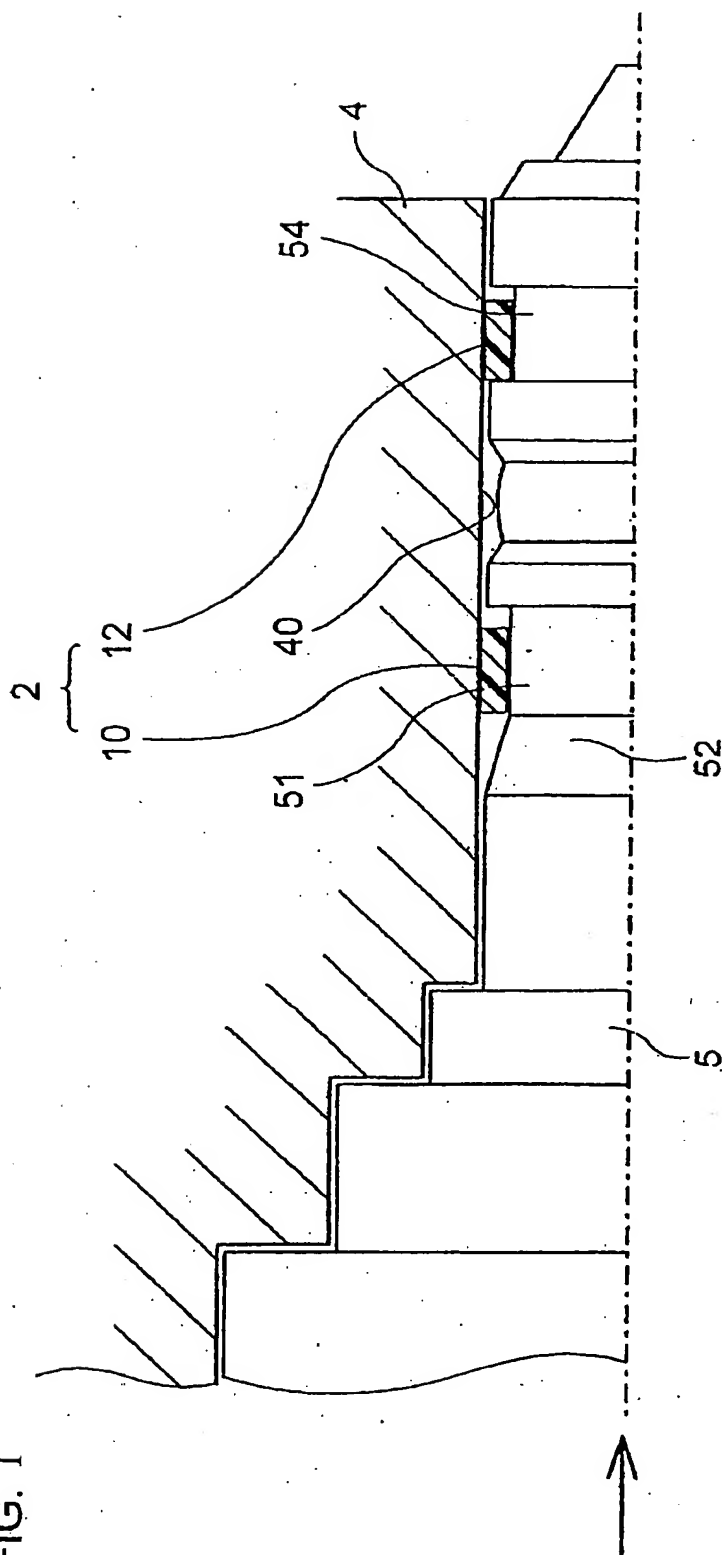
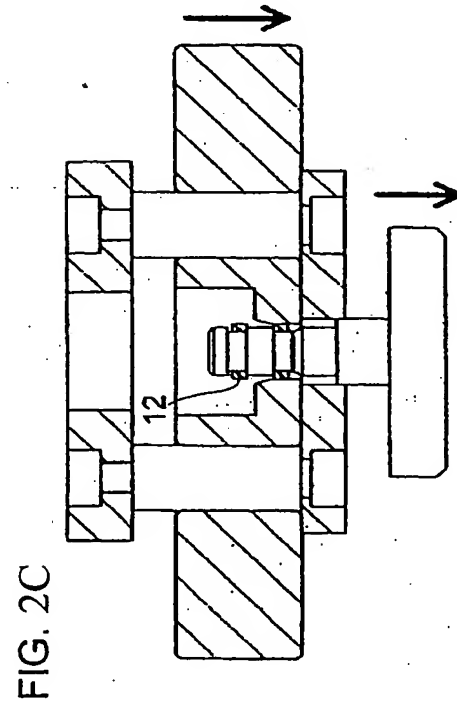
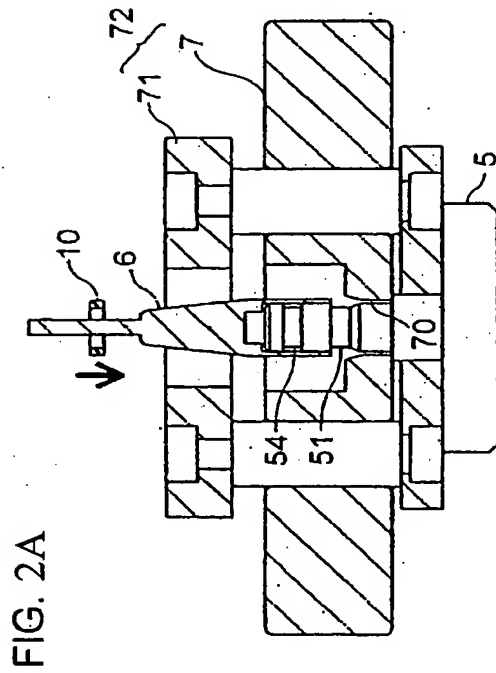
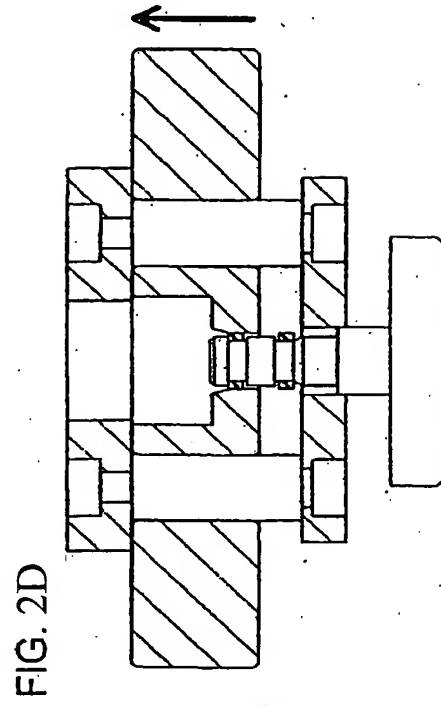
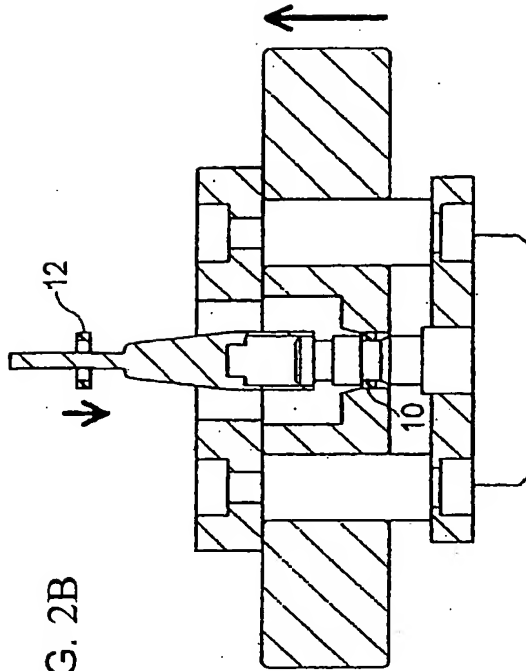


FIG. 1



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This cross-sectional view shows a semiconductor device. A gate stack, labeled 3, is positioned on a substrate 4. The gate stack includes a gate dielectric 10, a gate conductive layer 11, and a gate insulating layer 12. A trench 5 is formed in the substrate 4, with a gate conductive layer 11a and a gate dielectric 11b lining its side walls. A conductive layer 53 is deposited on the top surface of the gate stack 3 and the side walls of the trench 5. A conductive layer 54 is deposited on the top surface of the gate stack 3. A conductive layer 52 is deposited on the top surface of the gate stack 3. A conductive layer 51 is deposited on the top surface of the gate stack 3. A conductive layer 50 is deposited on the top surface of the gate stack 3. A conductive layer 40 is deposited on the top surface of the gate stack 3. A conductive layer 41 is deposited on the top surface of the gate stack 3. A conductive layer 39 is deposited on the top surface of the gate stack 3. A conductive layer 38 is deposited on the top surface of the gate stack 3. A conductive layer 37 is deposited on the top surface of the gate stack 3. A conductive layer 36 is deposited on the top surface of the gate stack 3. A conductive layer 35 is deposited on the top surface of the gate stack 3. A conductive layer 34 is deposited on the top surface of the gate stack 3. A conductive layer 33 is deposited on the top surface of the gate stack 3. A conductive layer 32 is deposited on the top surface of the gate stack 3. A conductive layer 31 is deposited on the top surface of the gate stack 3. A conductive layer 30 is deposited on the top surface of the gate stack 3. A conductive layer 29 is deposited on the top surface of the gate stack 3. A conductive layer 28 is deposited on the top surface of the gate stack 3. A conductive layer 27 is deposited on the top surface of the gate stack 3. A conductive layer 26 is deposited on the top surface of the gate stack 3. A conductive layer 25 is deposited on the top surface of the gate stack 3. A conductive layer 24 is deposited on the top surface of the gate stack 3. A conductive layer 23 is deposited on the top surface of the gate stack 3. A conductive layer 22 is deposited on the top surface of the gate stack 3. A conductive layer 21 is deposited on the top surface of the gate stack 3. A conductive layer 20 is deposited on the top surface of the gate stack 3. A conductive layer 19 is deposited on the top surface of the gate stack 3. A conductive layer 18 is deposited on the top surface of the gate stack 3. A conductive layer 17 is deposited on the top surface of the gate stack 3. A conductive layer 16 is deposited on the top surface of the gate stack 3. A conductive layer 15 is deposited on the top surface of the gate stack 3. A conductive layer 14 is deposited on the top surface of the gate stack 3. A conductive layer 13 is deposited on the top surface of the gate stack 3. A conductive layer 12 is deposited on the top surface of the gate stack 3. A conductive layer 11 is deposited on the top surface of the gate stack 3. A conductive layer 10 is deposited on the top surface of the gate stack 3. A conductive layer 9 is deposited on the top surface of the gate stack 3. A conductive layer 8 is deposited on the top surface of the gate stack 3. A conductive layer 7 is deposited on the top surface of the gate stack 3. A conductive layer 6 is deposited on the top surface of the gate stack 3. A conductive layer 5 is deposited on the top surface of the gate stack 3. A conductive layer 4 is deposited on the top surface of the gate stack 3. A conductive layer 3 is deposited on the top surface of the gate stack 3. A conductive layer 2 is deposited on the top surface of the gate stack 3. A conductive layer 1 is deposited on the top surface of the gate stack 3. A conductive layer 0 is deposited on the top surface of the gate stack 3.